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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/550,645	08/23/2006	Tominaga Koji	FUJ0002US	1944

23413 7590 09/14/2009

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EXAMINER	
MALEK, MALIHEH	
ART UNIT	PAPER NUMBER
2813	

NOTIFICATION DATE	DELIVERY MODE
09/14/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

usptopatentmail@cantorcolburn.com

Office Action Summary	Application No.	Applicant(s)	
	10/550,645	KOJI ET AL.	
	Examiner	Art Unit	
	MALIHEH MALEK	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05/05/2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/22/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendments filed on 05/05/2009. Claims 1-6 are pending in this application. Applicant amended claims 3, 4, 5 and 6.

Claim Objections

1. Claims 3 and 6 are objected to as containing the following minor informalities:

- In claims 3 and 6, line 3, the recitation "*insulating film the same as*" appears to be "*insulating film is the same as*"

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in **Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966)**, that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: ***(See MPEP Ch. 2141)***

a. Determining the scope and contents of the prior art;
b. Ascertaining the differences between the prior art and the claims in issue;
c. Resolving the level of ordinary skill in the pertinent art; and
d. Evaluating evidence of secondary considerations for indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly

owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cabral, JR. et al. (Pub. No.: US 2006/0138603 A1), herein Cabral, in view of Doh et al. (Pub. No.: US 2006/0115993 A1 or KR 02-54606), herein Doh.

Regarding claim 1, Cabral teaches a semiconductor device comprising a silicon substrate; an interface layer provided on the silicon substrate, the interface layer comprising a metal silicate; a diffusion suppressing layer provided on the interface layer; and a high dielectric constant insulating film provided on the diffusion suppressing layer ([0077], "…*other suitable lower layer materials include metal oxides or* ***metal silicates****. A* ***high-K dielectric layer*** *56 selected from the group consisting of* ***hafnium oxide*** *and/or zirconium oxide…the dielectric materials comprising the multilayer structure with hafnium oxide and/or zirconium oxide are selected from the group including, but not limited to:* Ta_2O_5, TiO_2, ZrO_2, HfO_2, Al_2O_3, La_2O_3, Y_2O_3, *yttrium alumnate, lathnaum alumnate, lanthanum silicate, yttrium silicate,* ***hafnium silicate****, zirconium silicate, doped or undoped mixtures, layers or* ***combinations thereof****…,*" and [0088]).

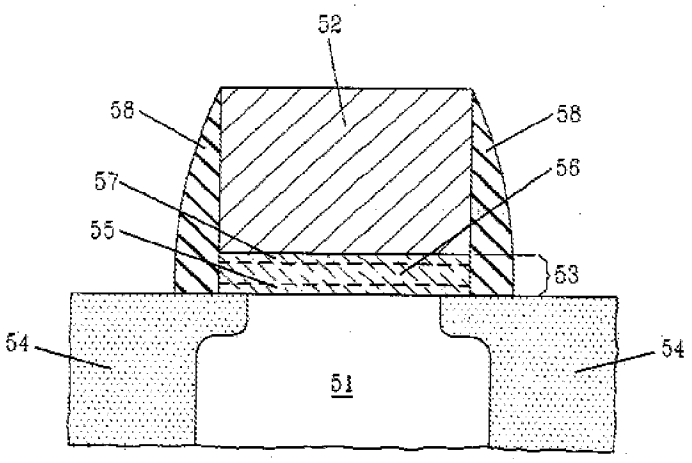


FIG. 14

However, regarding claim 1, Cabral does not explicitly teach a diffusion suppressing layer provided on the interface layer.

In the same field of endeavor, regarding claim 1, Doh teaches a diffusion suppressing layer provided on the interface layer ([0006]-[0009], "*...In various embodiments of the present invention, a method for treating one or more high dielectric layers of one or more integrated circuit devices involves the nitriding of a silicon substrate upon which the high dielectric layer is formed. The nitriding of the substrate may be performed, for example, by using a nitrogen plasma treatment, a thermal treatment in a nitrogen atmosphere, or* ***a thermal treatment of a nitrogen layer formed on the substrate****. Following nitriding, the silicon substrate and high dielectric layer are post treated by oxidizing the substrate to which the nitriding was applied, annealing the substrate to which the nitriding was applied, or by both oxidizing and annealing the substrate to which the nitriding

was applied,") to form high dielectric layers having superior mobility and interfacial characteristics (abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Cabral by incorporating the diffusion suppressing layer of Doh to form high dielectric layers having superior mobility and interfacial characteristics (Doh, abstract).

Regarding claim 3, Cabral teaches a semiconductor device wherein a high dielectric constant metal constitutional element of the high dielectric constant insulating film is the same as a high dielectric constant metal constitutional element of the interface layer to prevent a reaction between the adjacent layers ([0077] and [0088]).

4. Claims 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cabral, JR. et al. (Pub. No.: US 2006/0138603 A1), herein Cabral, in view of Doh et al. (Pub. No.: US 2006/0115993 A1 or KR 02-54606), herein Doh, as applied above, and further in view of Bai (Pub. No.: US 2001/0013629 A1).

Regarding claim 2, the previous combination remains as applied to claim 1 above.

However, regarding claim 2, the previous combination does not teach a semiconductor device wherein the interface layer has an equivalently converted SiO_2 thickness of 1.0 nm or smaller.

In the same field of endeavor, regarding claim 2, Bai teaches a semiconductor device wherein the interface layer has an equivalently converted SiO_2 thickness of 1.0 nm or smaller ([0020] and table I) to increase the capacitance of a gate dielectric without decreasing the performance of the device ([0012]). Bai discloses the claimed invention except for the exact value of the SiO_2 thickness of 1.0 nm or less. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have an interface layer having equivalently converted SiO_2 thickness of 1.0 nm or less, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller, 105 USPQ 233 (CCPA 1955).*

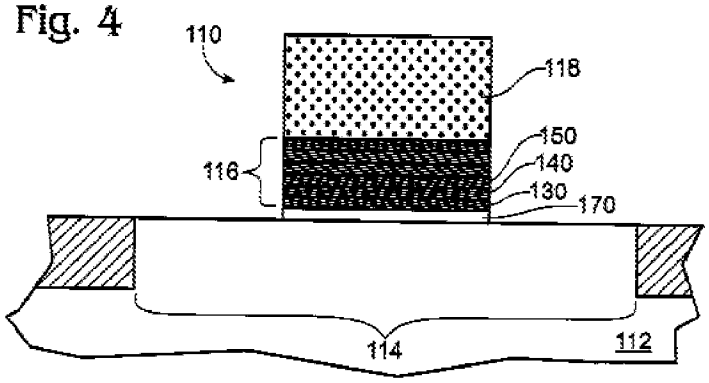
Regarding claim 6, Harada teaches a semiconductor device wherein a high dielectric constant metal constitutional element of the high dielectric constant insulating film is the same as a high dielectric constant metal constitutional element of the interface layer to prevent a reaction between the adjacent layers ([0075]).

5. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. (Pub. No.: US 2002/0130340 A1), herein Ma, in view of Harada (Pub. No.: US 2002/0195643 A1).

Regarding claim 4, Ma teaches a method for manufacturing a semiconductor device, comprising: forming, on one surface of a silicon substrate

112, an initial layer 140 which is a high dielectric constant metal element film for being mutually diffused with silicon in the silicon substrate; forming a diffusion suppressing layer 130 on the surface of the initial layer; performing heat treatment to allow the high dielectric constant metal element film of the initial layer to be mutually diffused with silicon in the silicon substrate, thereby forming an interface layer comprising a metal silicate; and forming a high dielectric constant insulating film 140 on the surface of the diffusion suppressing layer, wherein the diffusion suppressing layer comprises nitrogen (Figs. 3-4).

Fig. 4



Regarding claim 4, Ma, in paragraphs [0034]-[0035], teaches that "*it would also be possible to reverse the order of the materials such that high-k layer 140 would be deposited prior to interposing layer 130,*" and "*if high-k layer 140 would otherwise be in contact with the underlying silicon substrate, an oxidation barrier 170 is provided between the substrate 112 and multilayer dielectric stack 116… where the layer 170 includes silicon nitride or silicon oxynitride*." Therefore, Ma teaches forming the initial layer 140 which is a high dielectric constant metal film on one surface of the silicon substrate (e.g. hafnium oxide, see [0033]), and forming a diffusion suppressing layer 130 on the surface of the initial layer,

wherein the diffusion suppressing layer comprises nitrogen (aluminum nitride or silicon nitride, as explained in paragraph [0033]). Ma further, in paragraph [0049], teaches "*step 550 is the annealing of the multilayer dielectric stack in … **a mixture of nitrogen and hydrogen**, or ... the annealing is preferably performed at an elevated temperature of between 400 and 900 degrees Celsius to condition the high-k layers and the interposing layers as well as the interfaces between the various layers and **the interface with the underlying silicon**.*"

However, Ma does not expressly teach "a high dielectric constant metal element for being mutually diffused with silicon in the silicon substrate" and "…to allow the high dielectric constant metal element film of the initial layer to be mutually diffused with silicon in the silicon substrate, thereby forming an interface layer comprising a metal silicate."

In the same field of endeavor, regarding claim 4, Harada, in figures 9A-9D and paragraphs [0113]-[0115], teaches forming the layer 21B (SiON) and the layer 22A (HfO_2) on the silicon substrate, and "*a heat treatment (PDA: post deposition anneal) is performed with respect to the HfO_2 film 22A. PDA is performed, for example, in a nitrogen atmosphere at about 700 ºC for 30 seconds. Now, changes occurring in the stacked structure of the SiON film 21B and the HfO_2 film 22A by performing PDA will be described in detail with reference to FIGS. 9A to 9D. As described above, before performing PDA, as shown in FIG. 9A, the SiON film 21B and the HfO_2 film 22A contain hydrogen. When PDA is performed, as shown in FIG. 9B, hydrogen is desorbed from the*

SiON film 21B and the HfO_2 film 22A efficiently in the form of hydrogen gas. As a result, as shown in FIG. 9C, vacancies (white circles in FIG. 9C) are formed in the SiON film 21B and the HfO_2 film 22A. Then, as shown in FIG. 9D, ***silicon contained in the silicon substrate 20 or the SiON film 21B is diffused into the HfO_2 film 22A through the vacancies****, and* ***Hf contained in the HfO_2 film 22A is diffused into the SiON film 21B****. As a result, as shown in FIG. 7C, a silicon-containing HfO_2 film 22 having high thermal stability is formed, and a lower barrier film 21 made of the Hf-containing SiON film having a high relative dielectric constant can be formed. The silicon-containing HfO_2 film 22 is formed by making the HfO_2 film 22A dense by the diffusion of silicon. The specific composition of the lower barrier film 21 is the same as the lower barrier film 11b of the first embodiment. In other words, vacancies obtained by desorbing hydrogen from the HfO_2 film 22A and the SiON film 21B has the effect of promoting mutual diffusion of Hf and Si. In this case, setting the temperature for PDA to about 700 ºC brings about double effects, that is, an effect of promoting hydrogen desorption to facilitate formation of vacancies and an effect of facilitating diffusion of Hf or Si…, and consequently the relative dielectric constant of the gate insulating film 25 as a whole can be increased*."

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made forming, on one surface of a silicon substrate, an initial layer 140 which is a high dielectric constant metal element film for being mutually diffused with silicon in the silicon substrate; forming a diffusion

suppressing layer 130 on the surface of the initial layer; performing heat treatment to allow the high dielectric constant metal element film of the initial layer to be mutually diffused with silicon in the silicon substrate, thereby forming an interface layer comprising a metal silicate; and forming a high dielectric constant insulating film 140 on the surface of the diffusion suppressing layer, wherein the diffusion suppressing layer comprises nitrogen.

Regarding claim 5, applicant is referred to the rejection applied to claim 4 above. Furthermore, Ma teaches that the number and pattern of the layers in stack 116 could repeat many times; therefore it is obvious that the heat treatment is performed for some of the layers before and for the others after the high dielectric constant layer formation. Applicant is also noted that performing heat treatment after or before forming the high dielectric constant insulating film is an obvious alternative since selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results; *In re Burhans, 154 F.2d 690 USPQ 330 (CCPA 1946); In re Gibson, 39 F2d 975, 5 USPQ 230 (CCPA 1930). MPEP 2144.04.*

Response to Arguments

6. Applicant's arguments, regarding claims 1-3, filed on 05/05/2009 have been fully considered but they are not persuasive.

- Regarding claim 1, applicant argues that the cited references do not teach or suggest a diffusion suppressing layer provided on the interface layer.

In response to applicant's argument, Cabral, in figure 14, teaches the stack 53 comprising the lower layer 55 which comprises metal silicate, the high-k dielectric layer 56 that comprises HfO_2, and the upper layer 57 that comprises a material selected from the group consisting of oxidized or nitrided surface of the middle layer, SiO_2, SiON, SiN, HfO_2 or Al_2O_3. Therefore, Cabral teaches a semiconductor device comprising: a silicon substrate; an interface layer 55 provided on the silicon substrate, the interface layer comprising a metal silicate; and a high dielectric constant insulating film 56. However, Cabral does not expressly teach a diffusion suppressing layer provided on the interface layer. In the same field of endeavor, Doh, in paragraphs [0006]-[0009], teaches "…*in various embodiments of the present invention, a method for treating one or more high dielectric layers of one or more integrated circuit devices involves the nitriding of a silicon substrate upon which the high dielectric layer is formed. The nitriding of the substrate may be performed, for example, by using a nitrogen plasma treatment, a thermal treatment in a nitrogen atmosphere, or* ***a thermal treatment of a nitrogen layer formed on the substrate****. Following nitriding, the silicon substrate and high dielectric layer are post treated by oxidizing the substrate to which the nitriding was applied, annealing the substrate to which the nitriding was applied, or by both oxidizing and annealing the substrate to which the nitriding was applied*…" As explained above, Doh teaches a diffusion suppressing layer (i.e. SiN) on the silicon substrate prior to forming the HfO_2 layer. Therefore, it would have been obvious to one of ordinary skill in the art at

the time the invention was made to modify the semiconductor device of Cabral by incorporating Doh's diffusing suppressing layer between the metal silicate layer 55 and the high-k dielectric layer 56 of Cabral.

Applicant if further noted that claim 1 is a device claim and the arguments B in page 5 of the remarks, filed on 05/05/09, does not apply to a device claim, and as long as the structure shown by the references meets the claimed structure, it reads on it.

7. Applicant's arguments with respect to claims 4-6 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MALIHEH MALEK whose telephone number is (571)270-1874. The examiner can normally be reached on Mon-Fri, 8:30-6pm ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Landau can be reached on (571)272-1731. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

September 03, 2009

/M. M./
Examiner, Art Unit 2813

/W. David Coleman/
Primary Examiner, Art Unit 2823